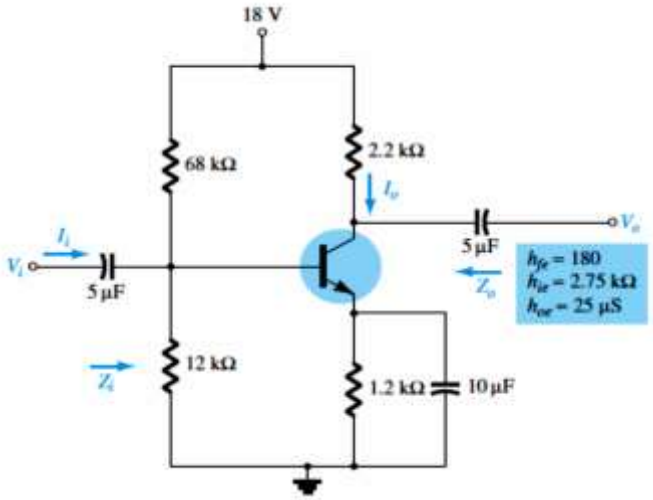
Nirma University
Institute of Technology
School of Engineering
Electrical Engineering Programme
2EE304: Analog and Digital Electronic Circuits

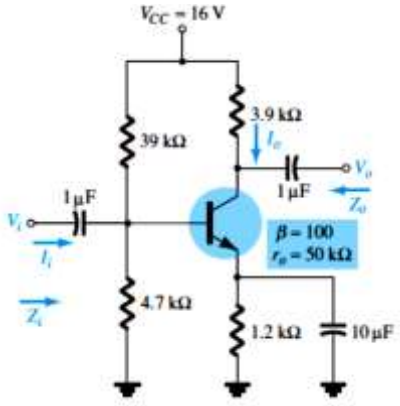
Assignment – 1

Issue Date: 13th September 2019 Submission Date: 19th September 2019

Q.1 For the network shown below:
a. Determine Z_i and Z_o .
b. Calculate A_v and A_i .
c. Determine r_e and compare βr_e to h_{ie} .



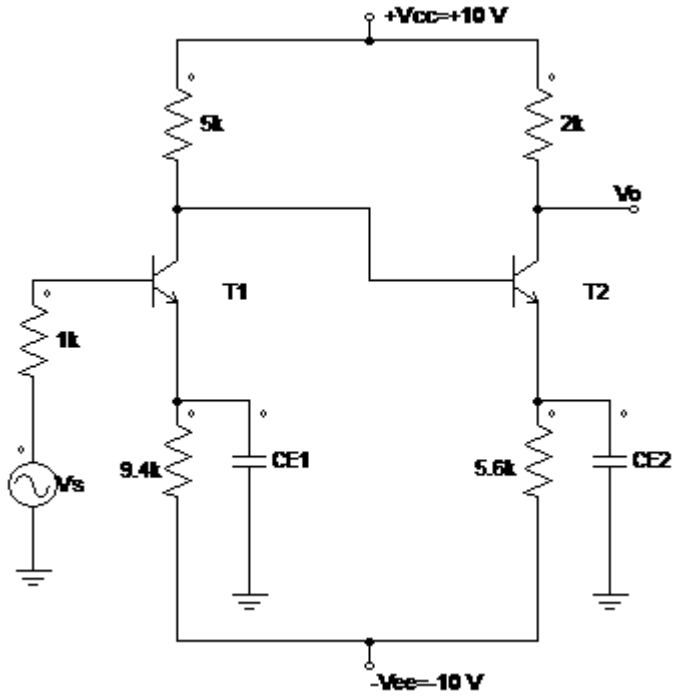
Q.2 For the network shown below :
a. Determine r_e .
b. Calculate Z_i and Z_o .
c. Find A_v.



Q.3 Explain the analysis of common emitter, emitter biasing circuit with and without bypass capacitor in r_e model and also derive voltage gain, current gain, input resistance and output resistance.

Q.4 Discuss the evolution of differential amplifier.

Q.5 For the given cascaded amplifier shown in figure, calculate Q-point of both transistors, input impedance, output impedance, overall gain and values of bypass capacitors. Take VBE=0.6 V and β=99.



Q.6 What is a level translator circuit? Why is it used with the cascaded differential amplifier?

Q.7 Prove that conventional amplifier follows exponential transfer characteristics whereas differential amplifier follows tanh transfer characteristics.

Q.8 Boolean function has minterms as 2,4,5,7,12,13,15,17,23,27,30 design the circuit by using K-map. Take 11 and 18 as don't cares.

Q.9 Prove that NAND and NOR gates are universal gates.

Q.10 Prove that SOP and POS forms of Boolean equations are inverse of each other by taking suitable example.

Q.11 Implement the full adder circuit and full subtractor circuit with NOR logic only.

Q.12 Design 16x1 multiplexer using two 8x1 multiplexers.

Q.13 Convert Active high SR latch into Active low SR Latch

Q.14 Discuss the applications of Multiplexers and De-Multiplexers

Q.15 Design a Logic Circuit of BCD to seven Segment display

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